What Is Claimed Is:

1. A data recovery circuit for recovering an m-bit data stream from an n-bit data stream, said data recovery circuit, comprising:

an n-bit data reconstruction circuit receiving said n-bit data stream, said n-bit data reconstruction circuit selecting a data boundary from a plurality of boundary selection candidates in response to a boundary selection signal and producing a reconstructed n-bit data stream based on said data boundary;

a first-in first-out (FIFO) buffer circuit coupled to an output of said n-bit data reconstruction circuit, said first-in first-out buffer circuit including a register and a write and read control circuit for controlling an n-bit write operation and an m-bit read operation of said register to receiving said reconstructed n-bit data stream and producing said m-bit data stream; and

a detection circuit coupled to an output of said FIFO buffer circuit, said detection circuit detecting said m-bit data stream and accordingly producing said boundary selection signal.

2. The data recovery circuit of claim 1, wherein n is a positive integer power of 2.

3. The data recovery circuit of claim 1, wherein n is smaller than m.

4. The data recovery circuit of claim 1, wherein m is not a multiple of n.

5. The data recovery circuit of claim 1, wherein said register having a number of bits equal to the least common multiple of n and m.

6. The data recovery circuit of claim 1, wherein a ratio of a transmission rate of said m-bit data stream to that of said n-bit data stream is n : m.

7. The data recovery circuit of claim 1, wherein said n-bit data reconstruction circuit comprises:

an input register for temporarily storing data from said n-bit data stream;

a data reconstruction multiplexer coupled to said input register, said data reconstruction multiplexer selecting said data boundary from said plurality of boundary selection candidates in response to said boundary selection signal and selecting reconstructed data from the data stored in said input register based on said data boundary; and

an output register coupled to said data reconstruction multiplexer, said output register temporarily storing the reconstructed data selected by said data reconstruction multiplexer and producing said reconstructed n-bit data stream.

8. The data recovery circuit of claim 1, wherein said detection circuit is incorporated in a decoder, which is operable to decode said m-bit data stream for output.

9. The data recovery circuit of claim 1, wherein said write and read control circuit comprises:

a write controller for controlling the n-bit write operation of said register and producing a write

pointer indicator signal; and

a read controller for controlling the m-bit read operation of said register based on said write pointer indicator signal.

10. A data receiving system, comprising:

a plurality of data recovery circuits, each for recovering one of a plurality of m-bit data streams from one of a plurality of n-bit data streams and decoding said one of a plurality of m-bit data streams into one of a plurality of decoded data streams, each of said data recovery circuit comprising:

an n-bit data reconstruction circuit receiving said n-bit data stream, said n-bit data reconstruction circuit selecting a data boundary from a plurality of boundary selection candidates in response to a boundary selection signal and producing a reconstructed n-bit data stream based on said data boundary;

a first-in first-out (FIFO) buffer circuit coupled to an output of said n-bit data reconstruction circuit, said first-in first-out buffer circuit including a register and a write and read control circuit for controlling an n-bit write operation and an m-bit read operation of said register to receiving said reconstructed n-bit data stream and producing said m-bit data stream; and

a decoder coupled to an output of said FIFO buffer circuit, said decoder including a detection circuit for detecting said m-bit data stream and accordingly producing said boundary selection signal, said decoder decoding said m-bit data

stream into said decoded data stream upon said detection circuit detects a correct condition of said m-bit data stream; and

a cycle alignment circuit receiving said plurality of decoded data streams from said plurality of data recovery circuits, said cycle alignment circuit aligning phases of said plurality of decoded data streams to synchronize said plurality of decoded data streams.

11. The data receiving system of claim 10, wherein said cycle alignment circuit comprises a plurality of delay lines, each for receiving one of said plurality of decoded data streams, each of said plurality of delay lines including a plurality of delay elements and a selector coupled to outputs of said plurality of delay elements to select one of said outputs of said plurality of delay elements as an aligned output.

12. A data recovery method for recovering an m-bit data stream from an n-bit data stream, said data recovery method comprising the steps of:

receiving said n-bit data stream;

selecting a data boundary from a plurality of boundary selection candidates in response to a boundary selection signal and producing a reconstructed n-bit data stream based on said data boundary;

performing an n-bit write operation to store said reconstructed n-bit data stream into a register and performing an m-bit read operation to retrieve said m-bit data stream from said register, a ratio of a rate of said write operation to that of said read operation being m : n; and

detecting whether or not said m-bit data stream conforms

to a predetermined format and accordingly producing said boundary selection signal.